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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Mark R. Thomann et al.	Examiner: Unknown	
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Title:	METHOD AND APPARATUS FOR A HIGH SPEED CYCLICAL REDUNDANCY CHECK SYSTEM		

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Please amend claim 8 as follows:

8. (Amended) A method for cyclical redundancy check error generation in a system having a cyclical redundancy check generator, a data latch, and a data buffer connected by a plurality of data bus lines, the data latch having a precharge circuit and the data buffer having data buffer outputs, the method comprising the steps of:

inhibiting the cyclical redundancy check generator and the data buffer outputs;

precharging the plurality of data bus lines to a first logic level until a cyclical redundancy check strobe is detected;

turning off the precharge circuit;

activating the data buffer outputs to modulate charge on the plurality of data bus lines;

waiting for a sufficient time for the plurality of data bus lines to develop a charge differential;

latching data on the plurality of data bus lines [on] in the data latch; and

performing a cyclical redundancy check on the data latched [by] in the data latch.

Please add claims 11-24 as follows:

11. (New) The method of claim 8, further comprising the step of isolating the data latch from the plurality of data bus lines after the data is latched in the data latch.

12. (New) The method of claim 8, wherein the step of inhibiting the cyclical redundancy